



GENERAL DESCRIPTION

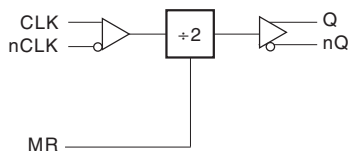


The ICS87332I-01 is a high performance ÷2 Differential-to-2.5V/3.3V ECL/LVPECL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The CLK, nCLK pair can accept most standard differential input levels. The ICS87332I-01 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS87332I-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

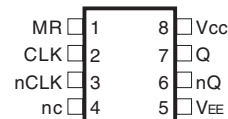
FEATURES

- One ÷2 differential 2.5V/3.3V LVPECL / ECL output
- One CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 500MHz
- Maximum input frequency: 1GHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Part-to-part skew: 400ps (maximum)
- Propagation delay: 1.6ns (maximum)
- LVPECL mode operating voltage supply range: $V_{CC} = 2.375V$ to $3.8V$, $V_{EE} = 0V$
- ECL mode operating voltage supply range: $V_{CC} = 0V$, $V_{EE} = -2.375V$ to $-3.8V$
- $-40^{\circ}C$ to $85^{\circ}C$ ambient operating temperature
- Lead-Free package fully RoHS compliant

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS87332I-01

8-Lead SOIC

3.90mm x 4.90mm x 1.37mm package body

M Package

Top View



TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|--------|-----------------|--------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | MR | Input | Pulldown | Master reset. When LOW, outputs are enabled. When HIGH, divider is reset forcing Q output LOW and nQ output HIGH. LVCMOS / LVTTTL interface level. |
| 2 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 3 | nCLK | Input | Pullup | Inverting differential clock input. |
| 4 | nc | Unused | | No connect. |
| 5 | V _{EE} | Power | | Negative supply pin. |
| 6, 7 | Q, nQ | Output | | Differential output pair. LVPECL interface levels. |
| 8 | V _{CC} | Power | | Positive supply pin. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |

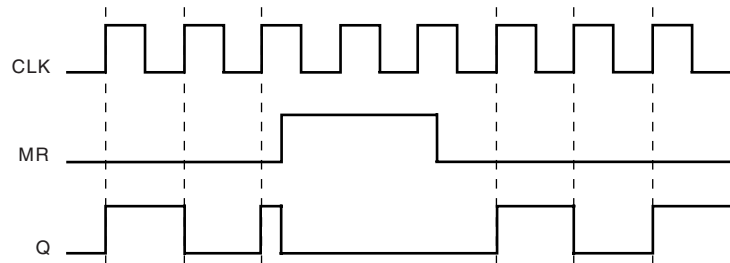


FIGURE 1. TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| | |
|------------------------------------------|--------------------------|
| Supply Voltage, V_{CC} | 4.6V |
| Inputs, V_i | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, I_o | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, θ_{JA} | 112.7°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = 2.375V$ TO $3.8V$, $V_{EE} = 0$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{CC} | Positive Supply Voltage | | 2.375 | 3.3 | 3.8 | V |
| I_{EE} | Power Supply Current | | | | 30 | mA |

TABLE 3B. LVCMOS DC CHARACTERISTICS, $V_{CC} = 2.375V$ TO $3.8V$, $V_{EE} = 0$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|------------------------------------|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | MR | 2 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | MR | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | MR $V_{CC} = V_{IN} = 3.8V$ | | | 150 | μA |
| I_{IL} | Input Low Current | MR $V_{CC} = 3.8V, V_{IN} = 0V$ | -5 | | | μA |

TABLE 3C. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = 2.375V$ TO $3.8V$, $V_{EE} = 0$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------------------------|-----------------|------------------------------|---------|-----------------|---------|
| I_{IH} | Input High Current | CLK | $V_{CC} = V_{IN} = 3.8V$ | | 150 | μA |
| | | nCLK | $V_{CC} = V_{IN} = 3.8V$ | | 5 | μA |
| I_{IL} | Input Low Current | CLK | $V_{CC} = 3.8V, V_{IN} = 0V$ | -5 | | μA |
| | | nCLK | $V_{CC} = 3.8V, V_{IN} = 0V$ | -150 | | μA |
| V_{PP} | Peak-to-Peak Input Voltage | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | $V_{EE} + 0.5$ | | $V_{CC} - 0.85$ | V |

NOTE 1: Common mode voltage is defined as V_{IH} .

NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is $V_{CC} + 0.3V$.



TABLE 3D. LVPECL DC CHARACTERISTICS, $V_{CC} = 2.375V$ TO $3.8V$, $V_{EE} = 0$, $T_A = -40^{\circ}C$ TO $85^{\circ}C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|----------------|---------|----------------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{CC} - 1.4$ | | $V_{CC} - 0.9$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{CC} - 2.0$ | | $V_{CC} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.65 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

TABLE 4. AC CHARACTERISTICS, $V_{CC} = 2.375V$ TO $3.8V$, $V_{EE} = 0$, $T_A = -40^{\circ}C$ TO $85^{\circ}C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|------------------------------|-----------------|---------|---------|---------|-------|
| f_{MAX} | Input Frequency | | | | 1 | GHz |
| t_{PD} | Propagation Delay; NOTE 1 | $f \leq 1GHz$ | 1.1 | 1.4 | 1.6 | ns |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 2, 3 | | | | 400 | ps |
| t_R | Output Rise Time | 20% to 80% | 200 | | 700 | ps |
| t_F | Output Fall Time | 20% to 80% | 200 | | 700 | ps |
| odc | Output Duty Cycle | | 49 | | 51 | % |

All parameters measured at 500MHz unless noted otherwise.

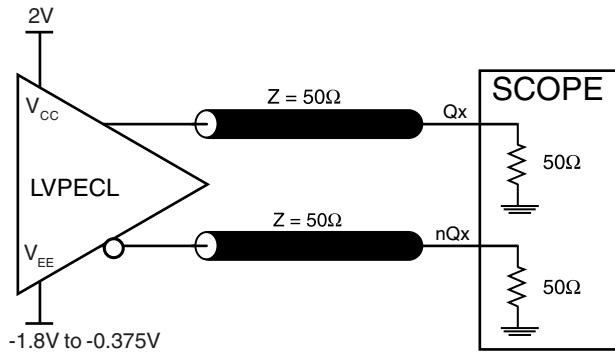
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

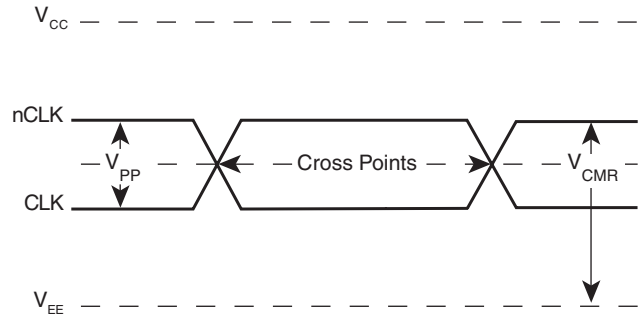
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.



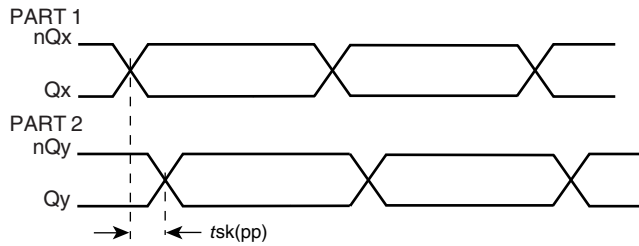
PARAMETER MEASUREMENT INFORMATION



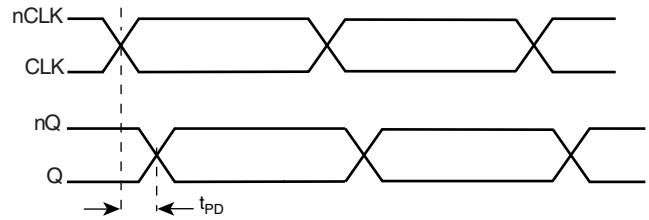
3.3V OUTPUT LOAD AC TEST CIRCUIT



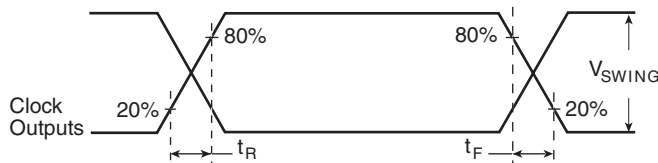
DIFFERENTIAL INPUT LEVEL



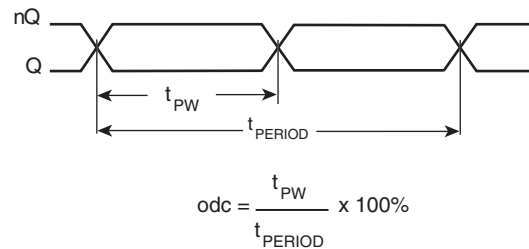
PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

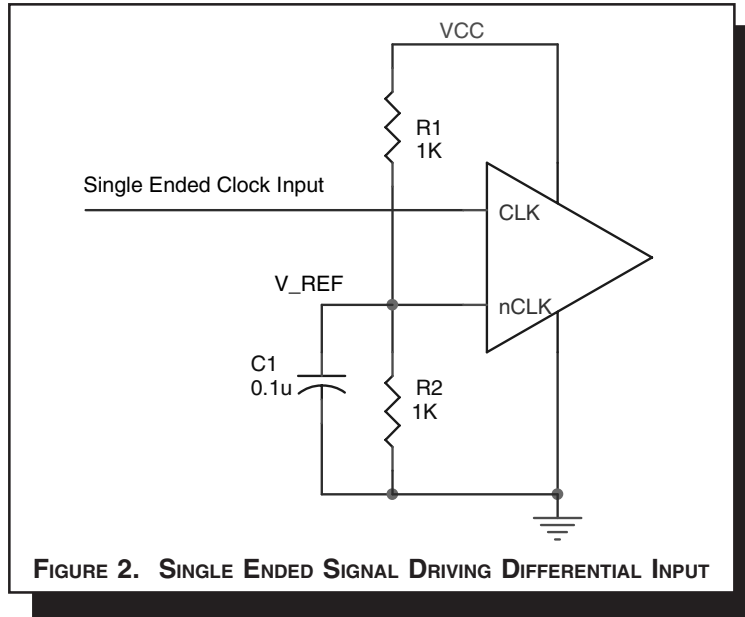


APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin.

of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

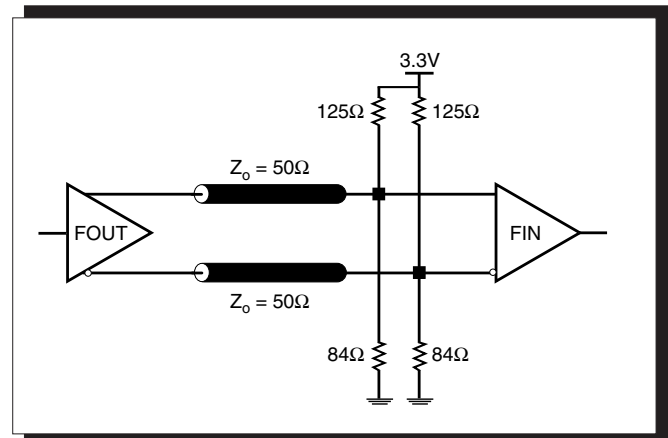
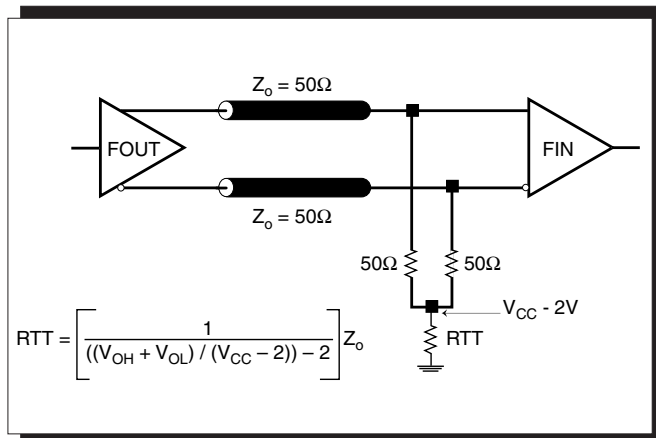


TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.





TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC} = 2.5V$, the $V_{CC} - 2V$ is very close to

ground level. The R3 in Figure 4B can be eliminated and the termination is shown in Figure 4C.

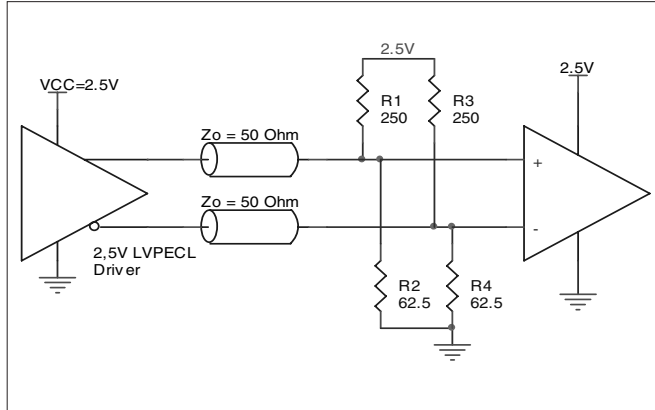


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

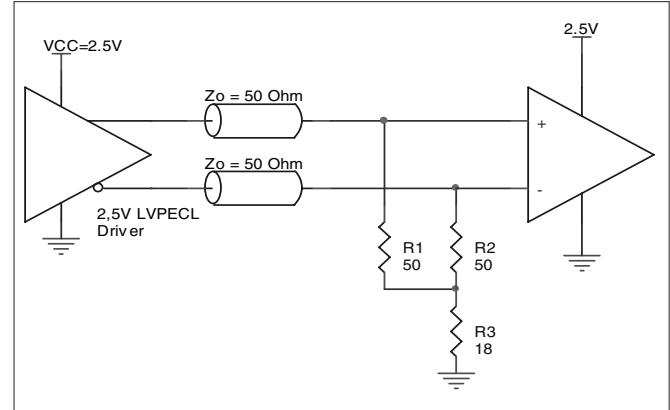


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

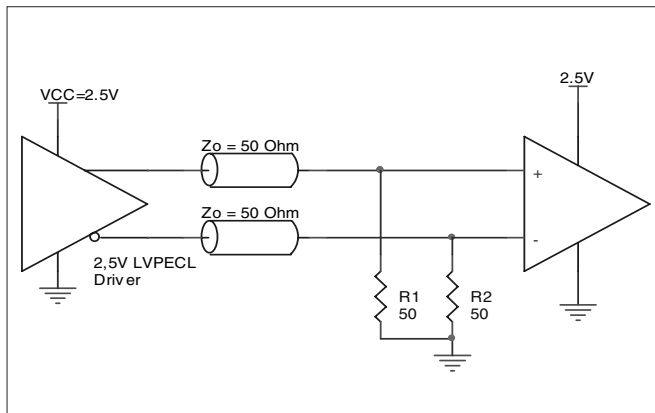


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE



DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 5A to 5E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 5A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

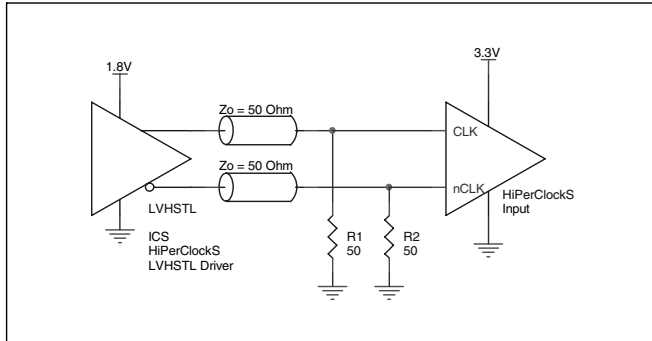


FIGURE 5A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER

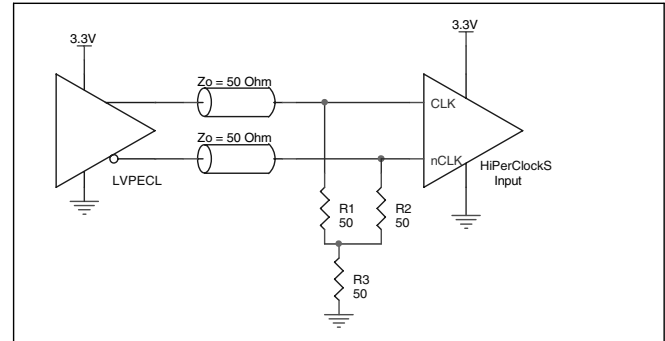


FIGURE 5B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

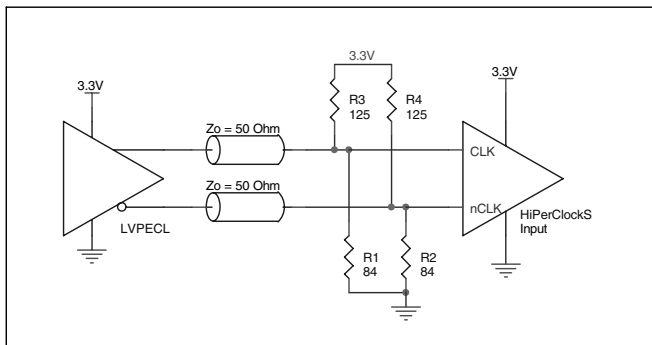


FIGURE 5C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

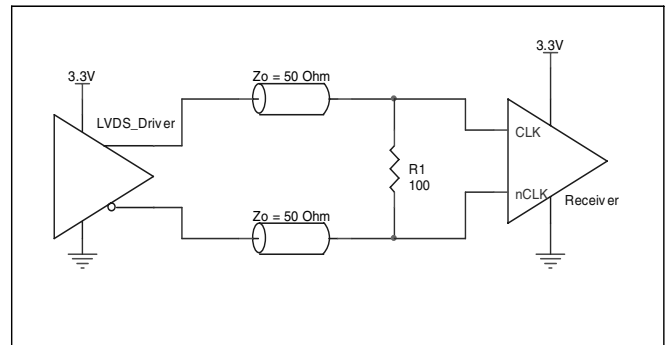


FIGURE 5D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

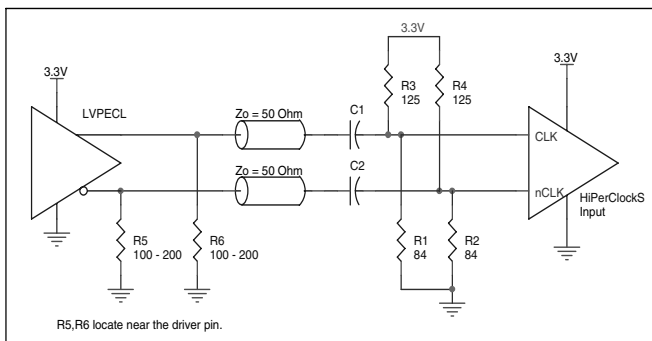


FIGURE 5E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS87332I-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS87332I-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.8V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.8V * 30mA = 114mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**

$$\text{Total Power}_{MAX} (3.8V, \text{ with all outputs switching}) = 114mW + 30mW = 144mW$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 5 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.144W * 103.3^\circ C/W = 99.9^\circ C. \text{ This is well below the limit of } 125^\circ C$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 5. THERMAL RESISTANCE θ_{JA} FOR 8-PIN SOIC, FORCED CONVECTION

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|----------------------------------------------------|-----------|-----------|-----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 153.3°C/W | 128.5°C/W | 115.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 112.7°C/W | 103.3°C/W | 97.1°C/W |

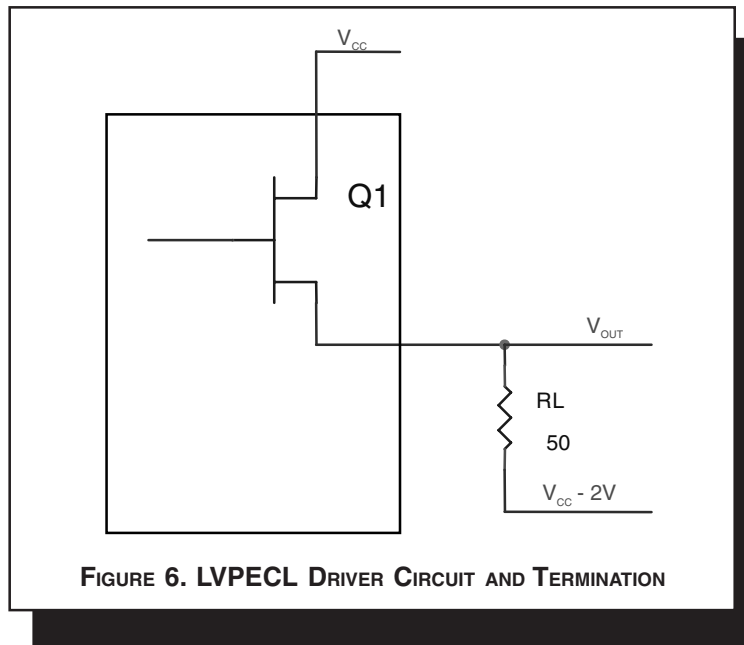
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.9V$
 $(V_{CC_MAX} - V_{OH_MAX}) = 0.9V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$
 $(V_{CC_MAX} - V_{OL_MAX}) = 1.7V$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = Pd_H + Pd_L = 30mW



RELIABILITY INFORMATION

TABLE 6. θ_{JA} vs. AIR FLOW TABLE

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|----------------------------------------------------|-----------|-----------|-----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 153.3°C/W | 128.5°C/W | 115.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 112.7°C/W | 103.3°C/W | 97.1°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87332I-01 is: 383

Compatible to part number MC100EP32



PACKAGE OUTLINE - M SUFFIX

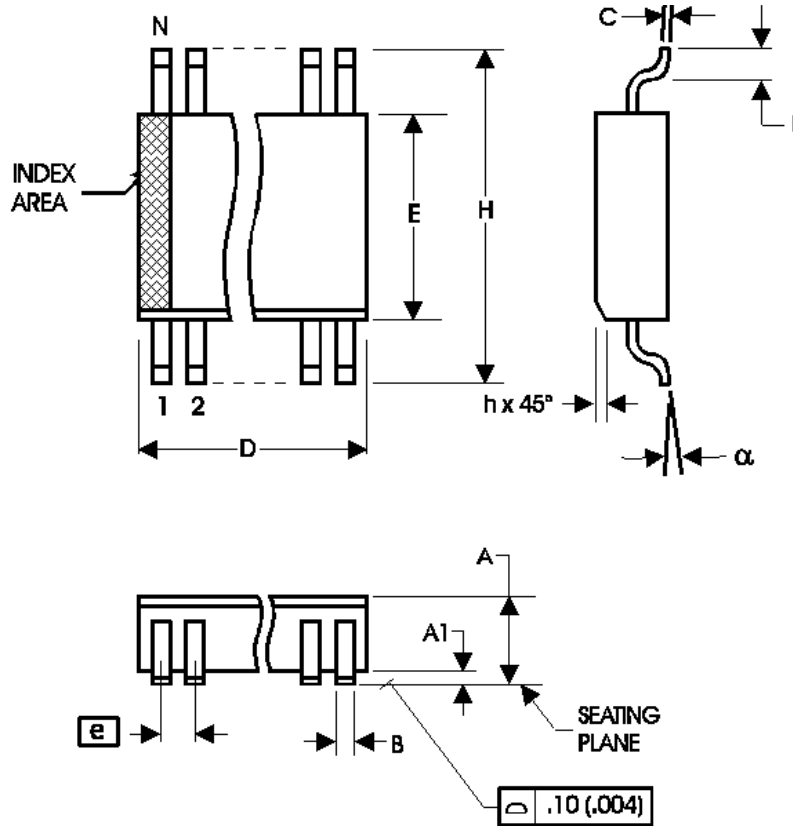


TABLE 7. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | MINIMUM | MAXIMUM |
| N | 8 | |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BASIC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |

Reference Document: JEDEC Publication 95, MS-012



Integrated
Circuit
Systems, Inc.

ICS87332I-01

÷2 DIFFERENTIAL-TO-2.5V/3.3V
ECL/LVPECL CLOCK GENERATOR

TABLE 8. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Package | Temperature |
|-------------------|----------|-------------------------|------------------|---------------|
| 87332AMI-01 | 7332AI01 | 8 lead SOIC | tube | -40°C to 85°C |
| 87332AMI-01T | 7332AI01 | 8 lead SOIC | 2500 tape & reel | -40°C to 85°C |
| 87332AMI-01LF | TBD | 8 lead "Lead-Free" SOIC | tube | -40°C to 85°C |
| 87332AMI-01LFT | TBD | 8 lead "Lead-Free" SOIC | 2500 tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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| REVISION HISTORY SHEET | | | | |
|------------------------|-----------------------------------------------------------------------------------------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------|---------|
| Rev | Table | Page | Description of Change | Date |
| B | T2 | 1 | Features Section - added Lead-Free bullet. | 7/5/05 |
| | | 2 | Pin Characteristics Table - changed CIN from 4pF max. to 4pF typical. | |
| | | 6 | Added "Wiring the Differential Input to Accept Single Ended Levels. | |
| | T8 | 6 | Added Termination for 3.3V LVPECL Output. | |
| | | 7 | Added Termination for 2.5V LVPECL Output. | |
| | | 8 | Added Differential Clock Input Interface. | |
| 13 | Ordering Information Table - corrected marking. Added Lead-Free part number and note. Updated format of datasheet. | | | |
| C | T3D | 4 | LVPECL DC Characteristics Table -corrected V_{OH} max. from $V_{CC} - 1.0V$ to $V_{CC} - 0.9V$; and V_{SWING} max. from 0.9V to 1.0V. | 4/13/07 |
| | | 9 - 10 | Power Considerations - corrected power dissipation to reflect V_{OH} max in Table 3D. | |
| | | | | |